REMARKS

The application has been reviewed in light of the Office Action dated December 22, 2004. Claims 1-6 have been rejected and pending.

Applicant wishes to thank the Examiner for indicating that claim 5 would be allowable if rewritten in independent from including all of the limitations of the base claim and any intervening claims. However, applicant has not elected to exercise this option as the claims stand allowable over prior arts.

Claims 1-4 and 6 stand rejected under 35 U.S.C. § 103 as being unpatentable over Williams (5,864,416) in view of Chorey (6,163,709).

The Office Action indicates that all features recited in base claim is disclosed by Williams, except the bit rate-recognition circuit has a structure of providing an extended range of recognizable total input voltages by connecting a plurality of logarithm amplifiers in series, each of which logarithm amplifier has a predetermined range of recognizable input voltage; however, such structures are well know in the art as shown by Chorey. Thus, one skilled in the art would have been motivated to employ the structure taught by Chorey in the bit rate recognition circuit of Williams. The applicant traverse this rejection for the following reason.

First, the Office Action indicates that the bit rate-sensing circuit of the present invention is shown, citing reference numeral 50 of FIG. 1 and as described in column 3, line 67 through column 4, line 5 in Williams. Williams indicates at column 3, line 67 through column 4, line 9 that "the present invention uses the data rate of the received signal **(known either a priori, or extracted by the phase lock loop of clock recovery circuit 50)**, to tune the operational bandwidth of the receiver, such that the upper end of the bandwidth (its upper 3dB) point is defined by the value of the transconductance g_m of the HJFET preamplifier stage 30 of the

transimpedance amplifier 20. Being able to set the maximum bandwidth of the receiver to a value that is no greater than is necessary for the data rate of the received signal serves to optimize the noise overall figure of the receiver". In addition, Williams at column 3, lines 60-65 reads "the operation of clock recovery circuit 50 is controlled via a control input 53 from control processor 100, either as a continuous sweep (in which **the control processor 100 instructs the receiver at what data rate the clock recovery circuit is sweeping**) or as **a predefined data rate selection mode**."

From the above page of Williams indicated cited by the Office Acton, one can not determine that a clock/data recovery circuit 50 outputs a sensing signal with a voltage level determined on the basis of a bit rate, as cited by the base claim 1. In Williams, since the control processor 100 outputs "digital code", its input must be in the form of the "digital code" (see column 4, lines 10-21). Applicant respectfully submit that such a "digital code" is clearly different from the "sensing signal with the voltage level predetermined on the basis of the bit rate" of base claim 1.

Secondly, the Office Action indicates that "a bit rate-recognition circuit for generating a recognition signal that is further amplified from the sensing signal" of base claim 1 is disclosed, citing reference numeral 50 in FIG. 1 as described in column 3. Applicant respectfully submit that the recognition signal that is amplified from the sensing signal is not outputted since the since the sensing signal with the voltage level predetermined on the basis of the bit rate is not outputted, as described above.

Thirdly, the Office Action indicates that a controller for determining a bit rate corresponding to a voltage level...by referring to a look up table of base claim 1 is disclosed by

Williams, citing column 4, lines 10-12 and reference numeral 53 of FIG. 1. More specifically, Williams teaches that "for this purpose, using a bandwidth control code look-up table previously stored in memory during a calibration phase of operation, **microcontroller 100 generates, either directly or interpolating between stored code values, an (eight bit) digital code representative of a control voltage to be output by digitally programmable current control circuit 40**. As described above, the control voltage generated by current control circuit 40 is applied to the drain resistor 35 at the control port 22 of transimpedance amplifier 20, so as to set the drain current supplied to FET 30, which in turn, sets its transconductance, and thereby the effective operational bandwidth of the amplifier." Thus, in Williams, the bit rate is determined by the clock/data recovery circuit 5, not the microcontroller 100. Also, unlike the present invention, the look-up table limits the relationship predetermined between the control voltage and the bit rate for controlling the transimpedance amplifier 20 in Williams. Moreover, in the case that the microcontroller 100 outputs the control signal that indicates the bit rate to the clock/data recovery circuit 50, the control signal is not a calculated value, but a pre-stored value, as in base claim 1.

Accordingly, Applicant respectfully submit that the Office Action wrongly equates the present invention with the features taught in Willaims.

Furthermore, Chorey, as read by applicant, relates to a transmitter for used in a cellular phone system. The RF detector 40 in Chorey (FIG. 4) is used to receive voice and data signals (Col. 8, lines 56-60). Further, the detector is used in a feedback control loop to control the power transmitted by the active power amplifier 4(Col. 9, lines 19-24). Therefore, Applicant disagrees

with the Office action assertion that Chrorey is in the same field of optical detectors which teaches the structure not shown in Williams.

The Court of Appeals for the Federal Circuit has stated that:

> The examiner must show reasons that the skilled artisan, **confronted with the same problems** as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed.

In Re Denis Rouffet, 47 USPQ.2d 1453, 1457-58 (Fed. Cir. 1998) (emphasis added).

The Office Action fails to meet this requirement. Nothing found in the reference cited in the Office Action addresses the **same problems** of the prior art solved by the present invention as defined in Claim 1. The features of Claim 1 address the need to a novel optical receiver that can easily adapt frequent changes in the transmission format and its bit rate, so that a real-time monitoring operation of the optical signals can be realized(see page 2, line17 through page 3, lines 5). Nothing found in Chorey address such a need.

> The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.

In re Fritch, 972 F.2d 1260, 1266, 23 USPQ 2d 1780, 1783-84 (Fed. Cir. 1992)

Moreover, the Office Action's reliance on the present inventions teaches is improper. See *In re Wertheim*, 191 USPQ 90, 102 (C.C.P.A. 1976) (Applicant's own disclosures cannot be used to support a rejection of the claims absent some admission that matter disclosed in the specification is in the prior art.).

In addition, the Federal Circuit has also stated:

> . . . rejecting patents solely by finding **prior art corollaries** for the claimed elements would permit an examiner to use the claimed invention itself as a **blueprint** for piecing together elements in the prior art to defeat the patentability of the claimed invention.

See *In Re Denis Rouffet.*

In the present situation, the Office Action appears to be using the claimed invention as a blueprint, which is improper. In particular, the Office Action has merely located references that may have use similar elements and has taken those terms out of context in attempt to piece together various elements using the present claims as a blueprint. This approach was specifically rejected in *Ex parte Clapp*, 227 USPQ 972, 973 (B.P.A.I. 1985):

> In the instant application, the examiner has done little more than cite references to show that one or more elements or subcombinations thereof, when each is viewed in a vacuum, is known. The claimed invention, however, is clearly directed to a combination of elements. That is to say, appellant does not claim that he has invented one or more new elements but has presented claims to a new combination of elements. To support the conclusion that the claimed combination is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed combination or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references

In order to establish a *prima facie* case of obviousness, the rationale to modify or combine the prior art must be expressly or impliedly contained in the prior art or reasoned from knowledge generally available to a person of ordinary skill in the art (*In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Applicant respectfully submits that such rationale is not present in the teachings of the references and thus the claims would not have been obvious to a person of ordinary skill in the art at the time of invention.

With regard to the possibility that the references could have been combined to result in a modification of the references as alleged, Applicant respectfully submit that it was held by the Court of Appeals in the case of *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ 2d 1780, 1783-84 (Fed. Cir. 1992) that:

> Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined *only* if there is some suggestion or incentive to do so. Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.

In the present case, it is respectfully submitted that the teachings of the combination of references do not overcome the standard of establishing obviousness as exemplified in *Fritch.*

Accordingly, it is respectfully submitted that the rejection of claims 1-4 and 6 should be withdrawn.

In light of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to kindly telephone the undersigned. If there are any fees due and owing, please charge Deposit Account No. 502-470.

Respectfully submitted,

CHA & REITER, LLC

By: _____
Steve S. Cha
Registration No. 44,069

Date: February 24, 2005

Mail all correspondence to:
Steve S. Cha, Reg. No. 44,069
CHA & REITER, LLC
210 Route 4 East, #103
Paramus, NJ 07652
Phone: (201)226-9245
Fax: (201)226-9246

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450 Alexandria, Va 22313-1450 on February 24, 2005.

Steve Cha, Reg. No. 44,069
(Name of Registered Representative)

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(Signature)